MJCE10-D0C-T1

Features

- Compliant with 100GBASE-LR4
- Up to 103.125 Gbps
- Integrated LAN WDM TOSA/ROSA for up to 10 km reach over SMF
- LC receptacle optical interface compliant
- No external reference clock
- Hot-pluggable
- Power dissipation < 3.5W
- Operating temperature range:
  0℃~+70℃
- RoHS Compliant
- DDMI function available with internally calibrated mode

Application

- Data Center
- 100GBASE-LR4 100G Ethernet

Standard

- Compliant with IEEE 802.3ba,IEEE802.3bm&100GLR4
- Compliant with SFF-8436
- RoHS Compliant

General Description

Mentech100G QSFP28 LR4 integrates four transmitter and receivers into one module. In the transmitter side, the four lanes of optical data channels are optically multiplexed by the integrated optical multiplexer. In the receive side, the four lanes of optical data channels are optically de-multiplexed by the integrated optical de-multiplexer. Each data channels is recovered by a PIN photo-detector and trans-impedance amplifier, retimed.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA) and compliant to IEEE 802.3bm

Specification

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Storage temperature	TS	-40	85	℃
Power Supply Voltage	Vcc	-0.5	+4	V
Relative Humidity	RH	5	95	%

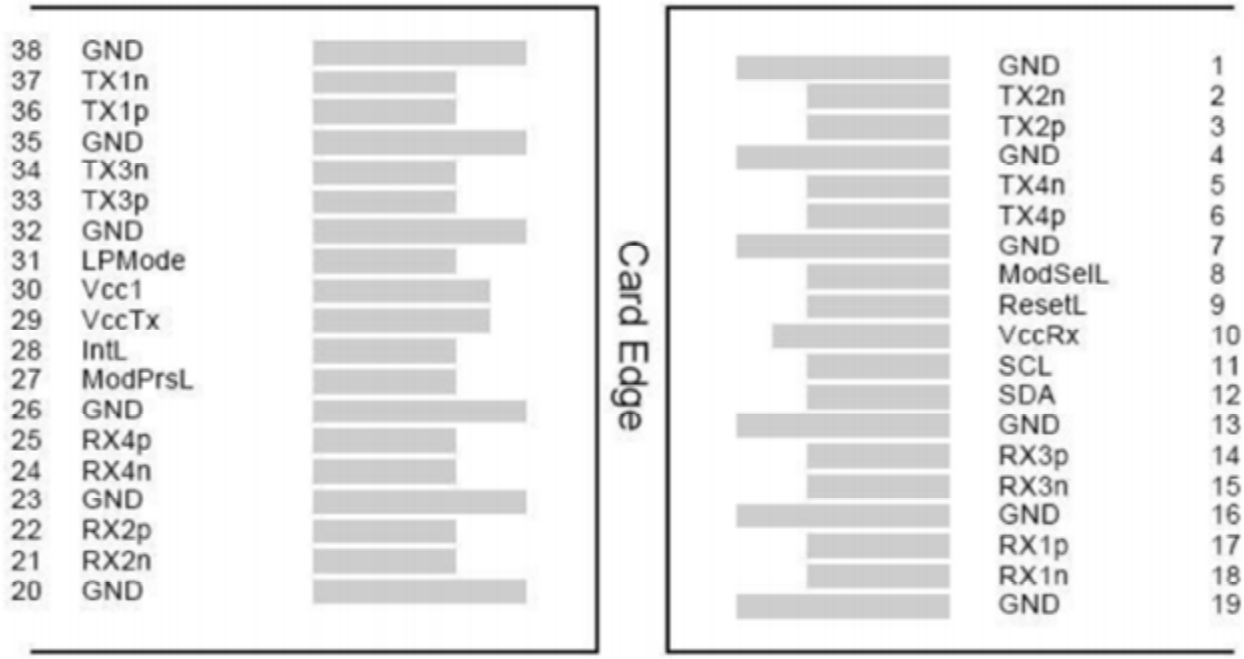
Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
Operating Case Temperature	Tc	0		70	℃
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Supply Current	Icc			1.12	A
Each Channel Data Rate	BR		25.78125		Gbps
SMF per G.652	Lmax	-	-	10	km

Electrical transmitter Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Signaling rate per lane		25.78125 ± 100 ppm			GBd	
Differential data input swing per lane				900	mV	
Differential termination mismatch				10	%	
Eye width			0.46		UI	
Eye height			95		mV	
DC common mode voltage		-350		2850	mV	
Electrical receiver Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Signaling rate per lane		25.78125 ± 100 ppm			GBd	
Differential data input swing per lane				900	mV	
Differential termination mismatch				10	%	
Eye width		0.57			UI	
Transition time, 20% to 80%	Tris/Tfall	12			ps	

Optical Transmitter Characteristics							
Parameter		**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Lane center wavelengths(range)			1294.53		1296.59	nm	
			1299.02		1301.09		
			1303.54		1305.63		
			1308.09		1310.19		
Total Average Launch Power		Pout			10.5	dBm	
Transmit OMA per Lane		TxOMA	-1.3		4.5	dBm	
Average Launch Power per Lane		TXPx	-4.3		4.5	dBm	
Extinction Ratio		ER	4			dB	
Sidemode Suppression ratio		SMSR	30			dB	
Relative Intensity Noise		RIN			-130	dB/Hz	
Transmitter Reflectance Reflectance					-12	dB	
Optical receiver Characteristics							
Parameter		**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Lane center wavelengths(range)			1294.53		1296.59	nm	
			1299.02		1301.09		
			1303.54		1305.63		
			1308.09		1310.19		
Average Receive Power per Lane		RXPx	-10.6		4.5	dBm	1，2，3
Receiver Sensitivity (OMA) per Lane		Rxsens			-8.6	dBm	
Receiver Reflectance					-26	dB	
LOS	Optical De-assert	Pd			-11.6	dBm	1
	Optical Assert	Pa	-24		-13.6		
LOS hysteresis			0.5		5	dB	1

Note1. Measured with a PRBS 2^{31}-1 test pattern, @25.78Gb/s, BER<10^{-12}, for each channel.
Note2. Minimum value is informative, equals min Tx OMA with infinite ER and max channel insertion loss.
Note3. Power value and power accuracy are with all channels on.

Pin Description



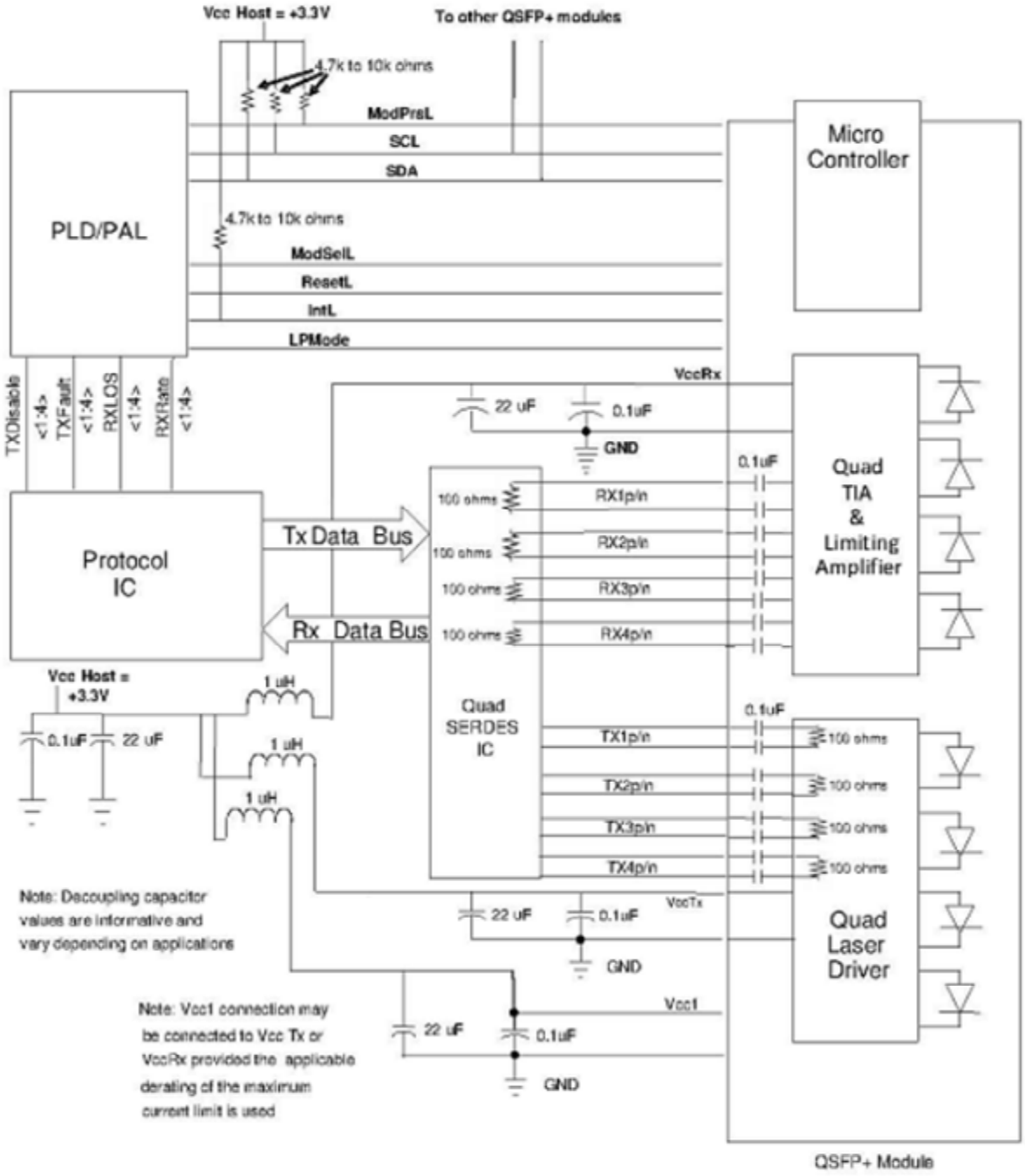
As Viewed Through Top of Board

Pin	Name	Function/Description	Note
1	GND	Ground.	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground.	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground.	
8	ModSelL	Module Select.	
9	ResetL	Module Reset.	
10	VccRx	3.3V Power Supply Receiver.	1
11	SCL	2-Wire serial Interface Clock.	
12	SDA	2-Wire serial Interface Data.	
13	GND	Ground.	
14	Rx3p	Receiver Non-Inverted Data Output.	
15	Rx3n	Receiver Inverted Data Output.	
16	GND	Ground.	
17	Rx1p	Receiver Non-Inverted Data Output.	
18	Rx1n	Receiver Inverted Data Output.	

19	GND	Ground.	
20	GND	Ground.	
21	Rx2n	Receiver Non-Inverted Data Output.	
22	Rx2p	Receiver Inverted Data Output.	
23	GND	Ground.	
24	Rx4n	Receiver Non-Inverted Data Output.	
25	Rx4p	Receiver Inverted Data Output.	
26	GND	Ground.	
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply.	1
30	Vcc1	3.3V power supply.	1
31	LPMode	Low Power Mode	
32	GND	Ground.	
33	Tx3p	Transmitter Inverted Data Input	
34	Tx3n	Transmitter Non-Inverted Data Input	
35	GND	Ground.	
36	Tx1p	Transmitter Inverted Data Input	
37	Tx1n	Transmitter Non-Inverted Data Input	
38	GND	Ground.	

Note1. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Typical application Circuit



Digital Diagnostic Functions

Mentech MJCE10-D0C-T1 support the 2-wire serial communication protocol as defined in the QSFP28 MSA. Which allows real-time access to the following operating parameters:

- temperature
- Received optical power
- Transmitter optical power
- Transmitter Bias
- Receiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alertend-users when particular operating parameters are outside of a factory-set normal range.

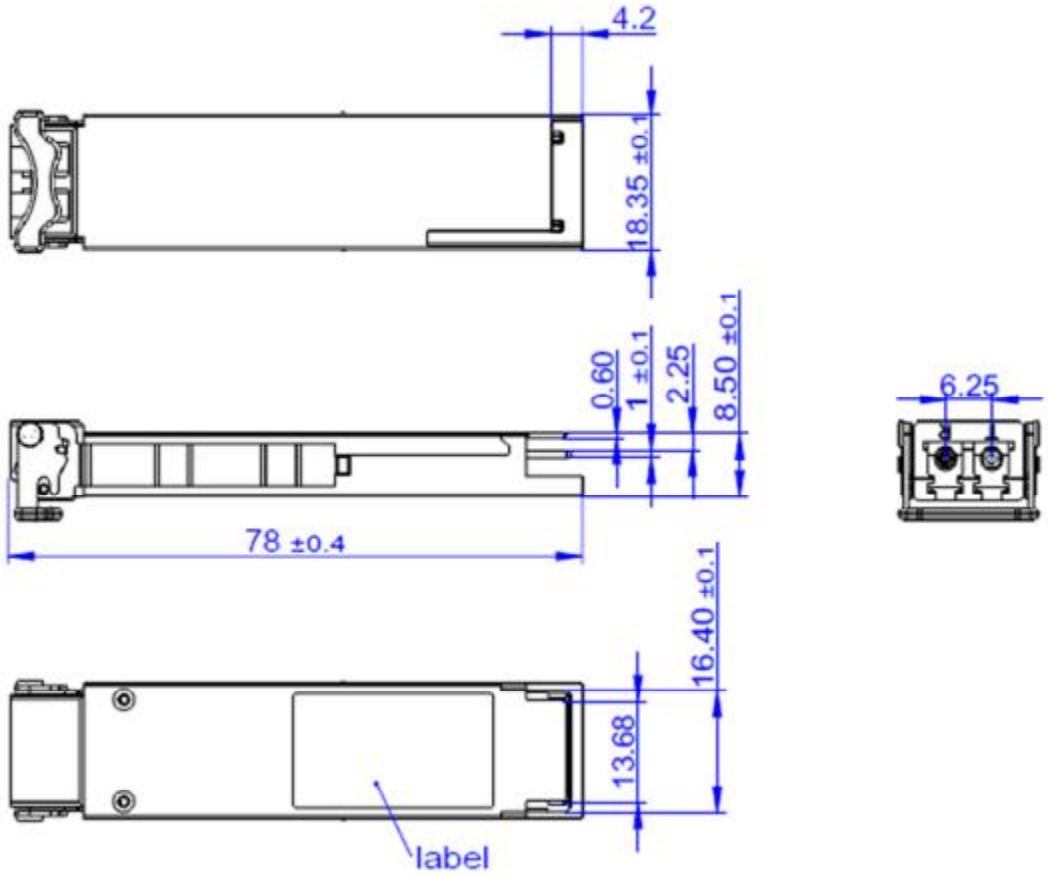
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Receiver Controller inside the Receiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 Receiver into those segments of its memory map that are no twrite-protected. The negative edge clocks data from the QSFP28Receiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP28 Receiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The structure of the memory is shown in Figure 2 -QSFP28 Memory Map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allow simple mentation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data Preliminary Page 7related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Package Outline

Dimensions are in millimeters. (Unit: mm)



Ordering information

Part. No		Specifications						
	Pack	Rate* (Gbps)	Po （dBm）	RX	Sen* (dBm)	Temp (℃)	Reach (km)	DDM
MJCE10-D0C-T1	QSFP28	25.78125	-1.3~-4.5	PIN	<-10.6	0~70	10	Y

*:For each channel.